Temperature effects on static behavior of the power JFET Normally-Off transistor based on 4H-SiC

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***Abstract*— In this work, the characterization and structural study of the normally-off JFET transistor based on 4H-SiC will be presented. We give the results performed on JFET SemiSouth transistor from the static characteristics (I_{DS}-V_{DS}) determined for temperatures between 27°C and 127 °C. At room temperature of 27°C the on state resistance was about 0.083Ω. It increased to 0.312 Ω for a temperature of 127 °C. The effect of temperature on the evolution of this resistance is discussed and compared to the one calculated using a mobility model.**

***Index Terms*—4H-SiC, Normally-off JFET, electrical characteristics, R_{DS_ON}.**

I. Introduction

The power JFET transistors are used in the on state in the linear regime. In this mode of operation for a N type JFET, the formed N channel ensures the conduction of the carriers between the source and the drain. When the transistor operates in the on state, it behaves as a resistor, notes R_{DS_ON}, which requires a drop voltage at the terminal of the component. This resistance is one of the most important parameters for a power component because it determines the losses conduction [1].

The studied vertical JFETs were manufactured by SemiSouth (SiC VJFETs). These transistors are dedicated for the power electronic applications and it were good candidates for use in high temperature environments. They combine the quick switching of the unipolar transistors (eg MOSFETs), the ability to switch high current densities and the excellent thermal properties of the silicon carbide materials [2, 3]. Thanks to the vertical channel structure, the SiC VJFETs allow a greater density of integration, very low state-on-resistance and easy manufacture process with low cost [4, 5]. Unlike the MOSFET, the SiC VJFET is based on the width modulation of the channel by the PN junction. Thus prevents degradation of the component to elevated temperatures of the gate oxide in MOSFETs case. The VJFETs are 100% unipolar; they can be easily connected in parallel to switch high current in the order of hundreds of amperes [4]. The majority of the power control systems require the mode "normally-off" so that the system is in a state "safe" even if the power control is interrupted [6].

II. Device Structure

SemiSouth's SiC VJFET (normally on or normally off) is based on a patented vertical-channel, trench structure, as given in Figure 1. This structure with a n–type channel can be described as follows: a substrate is a doped semiconductor layer n+, a channel n –type layer is located above the substrate, a p^+ -n junction is fabricated in the channel by means of ion implantation, a gate contact (ohmic) is formed on the p^+ -n junction. Finally a source and a gate contact (both ohmic) are formed on the n– type region, or channel.
The structure is built in a 4H-SiC epitaxial wafer with a 12µm- thick layer doped to n- = $7*10^{15}$ cm^{-3} capped by a heavily doped n+ > $1*10^{19}$ cm^{-3} layer. Deep trenches are dry-etched to facilitate implementation of the gating structure and blocking junction through three-step aluminum (Al) implantation.

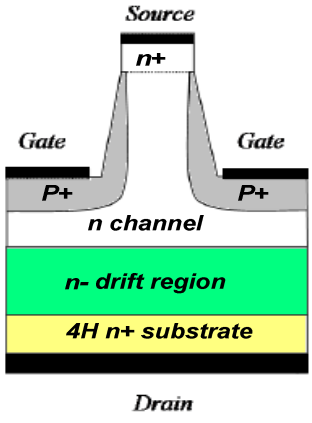

Fig. 1. Cross-section of SemiSouth's VJFET [7].

As seen in Fig. 1, the gate regions are created on the sidewalls of the trenches, resulting in 2.1 µm vertical junction

gates and a designed channel opening of 0.55 µm. Furthermore, the p^+ body regions are created under the trenches providing the p^+-n^- blocking junction at the depth of ~ 1µm from the trench bottom, yielding a blocking layer thickness of 9.4 µm when the p^+ implantation tail is considered. In addition, shallow, high concentration p^+ regions are created at the trench bottoms to facilitate the p-type gate contacts, which are placed at the centers of the trench bottoms. As seen in Fig. 1, the n-type source contacts are placed at the top surfaces of the mesa, and the drain contact on the substrate. The sidewalls of the trenches are passivity by a thermal oxide and silicon nitride, and the trenches are filled with a planarizing polyimide. The source contacts are connected by a metal overlay, which runs over the polyimide. In addition, the gate fingers are connected to a large bonding pad at one side of the device.

III. Results and Discussions

A. Linear region

In this region the expression of I_{DS} versus V_{DS} can be described by the equation (1) [8]:

$$I_{DS} = 2.\frac{I_{DSSAT}}{V_p^2}.\left[\left(V_{GS} - V_p\right) - \frac{V_{DS}^2}{2}\right] \quad (1)$$

Where V_p is the pinch-off voltage and I_{DSSAT} is the drain saturation current.

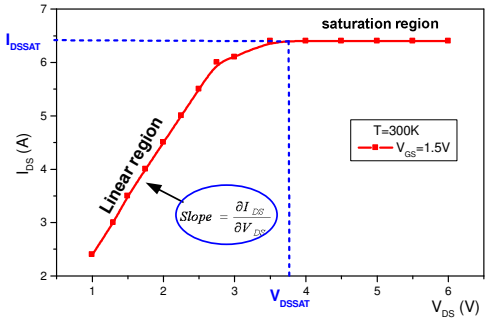

Fig. 2. The measured static characteristic showing the two operating zones.

B. Saturation region

In the saturation region, the dependence of the drain current I_{DS} versus V_{DS} can be written as:

$$I_{DS} = I_{DSS}.\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad (2)$$

I_{DS} is independent on V_{DS} at the saturation region, but the current increases for decreasing V_{GS}.

JFETs are non-linear transconductance devices with a characteristic approximated by a square law with the drain current I_{DS} dependent on the gate–source voltage V_{GS} [9]. Where I_{DSS} and V_p, respectively, characterize the maximum drain current saturation (where V_{GS} = 0) and the gate–source pinch-off voltage (where I_{DS}= 0).

The transfer characteristic, in saturation regime, is given by the variation of the drain source current I_{DS} as function of the bias voltage V_{GS}. This characteristic summarizes the limits of JFET: drain saturation current I_{DSS} for zero voltage of V_{GS}, and zero current for a drain voltage V_{GS} equal to the threshold voltage of V_{T0}.

The figure 3 shows the measurement of the I_{DS} current as a function of V_{GS} of the JFET, at room temperature 27°C and 127 ° C.

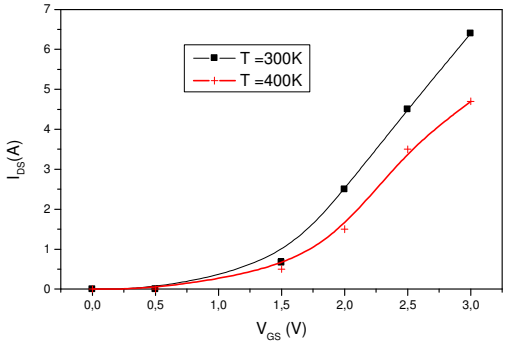

Fig. 3. The variation of the saturation current I_{DS} as function of V_{GS} at temperatures 300K and at 400K.

From these characteristics it can be noted that the drain source current varies nonlinearly as a function of V_{GS}. For a given temperature, the current increases when the V_{GS} vary from 0.5V to 3V. The reduction of the channel conduction width induces the decrease of I_{DS} current. It reach a zero corresponding to V_{GS}=V_{T0}. The threshold voltage decreases from 1.2V at 27°C to 0.9V at 127°C.

C. Electrical characterization of JFET-SiC

Fig.4 represented the used circuit to characterize the studied JFET transistor. It is formed around the IGBT transistor in switching mode. The Fig.5 shows the characteristics V_{DS} and I_{DS} as function of time, and from these curves we have been extracted point by point the static characteristics (V_{DS}, I_{DS}) given in figure 6 at different temperatures and V_{GS}.

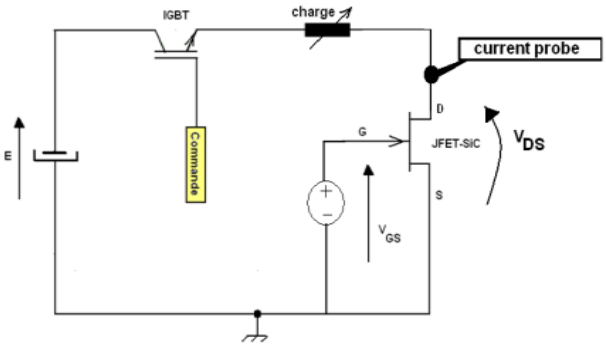

Fig. 4. Circuit used to determine the static characterization.

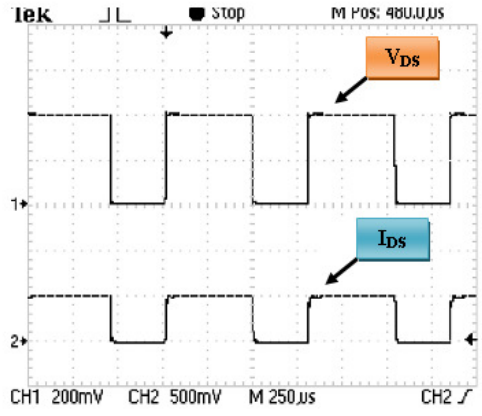

Fig. 5. The curves V_{DS} and I_{DS} as function of time.

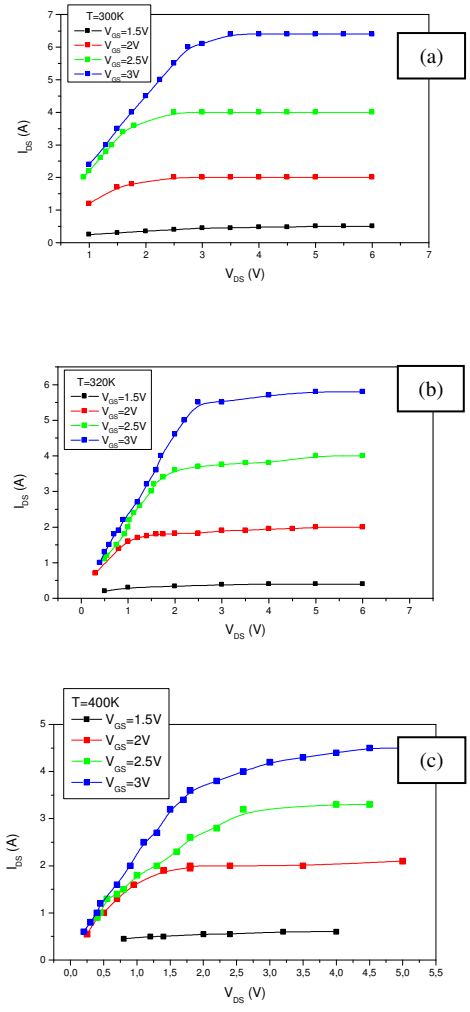

Fig. 6. The curves of drain-source current I_{DS} as function of drain-source voltage V_{DS} with different V_{GS} (a) at 300K (b) at T=360K and (c) at T=400K.

According to the preceding figures, we can observe the remarkable effect of temperature on the evolution of static characteristics (V_{DS}-I_{DS}) for different values of V_{GS}. From 27°C to 127°C, the drain source current decreases from 6.4A to 4.5A respectively.

From the linear region (ohmic zone) of the current-voltage characteristics of the JFET, we can deduce the on state resistance which represents the slope of the drain current with low V_{DS} [10]. This resistance can be expressed by equation (3):

$$R_{DS}^{ON} = \frac{1}{\frac{\partial I_{DS}}{\partial V_{DS}}(V_{DS} = 0, V_{GS} = 0)} \quad (3)$$

The equation 4 was used to determine the on-state specific resistance of n-type unipolar component [11, 12]:

$$R_{on,sp} = \frac{4V_{Br}^2}{\varepsilon.\mu_n E_C^3} = \frac{W_B}{q.\mu_n(T).N_D} \quad (4)$$

Where E_c is the critical field: (for 4H-SiC) is written according to the equation (5) cited by [13]. V_{Br} is the breakdown voltage given by (Eq. (6)) and depends on the doping density N_D (in the general case) and for the 4H-SiC this voltage is given by (eq. (7)), q is the elementary electron charge, ε=10 is the permittivity and μ is the electron mobility, it depends on the temperature and the doping concentration as mentioned by Moumen [14].

$$E_C(4H-SiC) = 3.3\times10^{14} N_D^{1/8} \quad (5)$$

$$V_{Br} = \frac{E_C.W_D}{2} = \frac{qN_D}{2\varepsilon}W_D^2 \quad (6)$$

$$V_{Br}(4H-SiC) = 3.0\times10^{15} N_D^{-3/4} \quad (7)$$

The mobility model is given by equation (8) [15, 16]:

$$\mu_n(T) = \frac{947}{1+\left(\frac{N_i}{1{,}94\times10^{17}}\right)^{0,61}}\left(\frac{T}{300}\right)^{-2,15} \quad (8)$$

Where N_i represents the total concentration of ionized impurities.

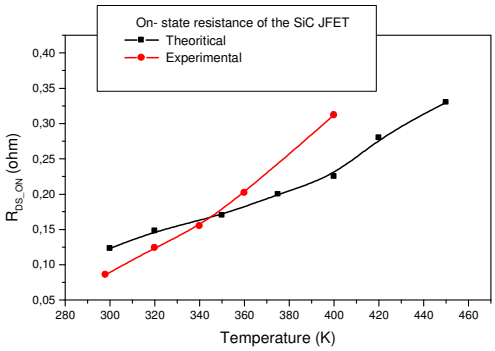

Fig. 7. The variation of the on-state resistance of the JFET-SiC.

The figure 7 illustrates the evolution of the experimental and theoretical on-state resistance of the JFET versus temperature. The experimental curve is derived from preceding static characteristics (V_{DS}-I_{DS}) and using the formula given by the equation (3). The range of variation of this experimental resistance is between 0.086Ω and 0.312Ω when temperature varied from 300K to 400K. The theoretically curve was determined using combined formulas cited previously. The theoretical values are varied from 0.123Ω at 300K to 0.330Ω at 450K. In the two cases the R_{DS_ON} increases according to the temperature. This behavior is due to the temperature which causes the decrease of the mobility and thus the increase in the resistivity of a semiconductor [17, 18]. By against the high temperatures cause higher leakage currents, and therefore the threshold voltage of V_{T0} components decrease.

IV. Conclusion

By studying the on state behavior, the VJFET device has demonstrated a low specific on-resistance in the range 0.086Ω to 0.312Ω when the temperature increases from 300K to 400K. Due to the intrinsic properties of SiC, it shows a low specific state resistance and the capacity of operating at high temperatures. It is necessary to take into account physical and geometrical characteristics of the JFET to evaluate at best the performance of the on- state. Thus, it is clear that the on state resistance is a major parameter for the power electronics: it is low, the losses will be small. It is important to study the influence of this parameter on the dynamic behavior of this type of transistor.

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